REMARKS

1. Claims corrections

Applicant has amended and rearranged claims 1-12 as suggested in the "Allowable Subject Matter", section 8 of this Report.

2. Priority

At the present time the Applicant encloses a certified copy of the Canadian application as required by 35 U.S.C. 119(b).

3. Drawings and the brief description of the drawings

Claim 10 concerning the expert system was eliminated. Consequently, please also delete Figure 10 and the description of the expert system found in the section "Detailed Description of the Preferred Embodiments" at paragraphs [0101] to [0108].

The drawings must show every feature of the invention specified in the claims. To abide to this request and to maintain the same form of graphical presentation of all drawings, please replace the previously added Figure 11 with new Figures 10, 11 and 12. Also, please replace previously added description of Figure 10 with the description of the new figures. The applicant suggests introducing the following amended description of Figures 10, 11 and 12 at the place of eliminated description of the expert system:

"A second embodiment of the proposed VLSI device for implementing in hardware any multiple-output combinational target circuit defined by a group of logical sum-of-product equations, considers every single sum-of-products logical equations as an independent equation. Each independent equation needs a maximum of q modified cells C(k), where a modified cell C(k) is used for determining the logical value of a product term p(k) of an independent equation. If the same product term is an element of several independent sum-of-product equation, this product term must be implemented several times in hardware, using a modified cell C(k) for each equation where the product term is there.

Let's assume that for this second embodiment, a multiple output target combinational circuit has the following equation that gives one of the outputs (the same equation as used for Z in (1)):

$$Z = a.b + \bar{a}.\bar{b}.\bar{c} + \bar{c}.\bar{d} \qquad (8)$$

Fig. 10 demonstrates how the mask words and the product words are applied to the associated inputs (**a = 1, b = 1, c = 0, d = 1**) to provide the output of the considered independent equation (8). **Fig. 11** shows partially the second embodiment of the proposed VLSI device, the structure **41** implementing only the independent equation (8). Each independent equation uses q modified cell C(k) **42,** as shows in **Fig. 12**. The modified cell **42** has only the mask word register **32** and the product word register **33** connected to the associated combinational part, formed by AND gates **35**, EQUIVALENCE (XNOR) gates **36**, and AND gate **37**. In **Fig. 11** one and only one final OR gate **39** is used to determine the logical value of the single output of the independent equation. This second embodiment of the proposed VLSI device can be equally used to implement the sum-of-product logical equations that describe the combinational parts of sequential target circuits".

Figures **2A** and **2B** are amended as suggested by the Examiner. New Figures **10, 11** and **12** have been added and the drawings are renumbered. The replacement sheets are labeled "Replacement Sheet". In the description of the preferred embodiments, the name "logical summing circuit" is only another equivalent expression for "OR gates" and the name "equivalence gates" is only another equivalent expression for "XNOR gates". For consistency, the necessary corrections were made in the drawings using only the terms "OR gates" and "XNOR gates".

Appropriate changes were made to the "Description of the drawings" section. The descriptions of the new drawings are the following:

FIG. 10 is an example of how the mask word and the function word are applied to the input variables to provide the value of the single output according to the second embodiment of the invention;

FIG 11 shows the structure of a part of the VLSI circuit implementing an independent sum-of-product equation of a combinational circuit according to the second embodiment of the invention;

FIG 12 shows the structure of a modified basic cell C(k) according to the second embodiment of the invention.

Claim objections under 35 USC 112, 6th

The Applicant has corrected and/or eliminated the misspelling of words in Claims 8 and 9. Claim 10 was cancelled.

Claim 11 was cancelled and rewritten as new claim 15 without cumulative claiming and multiple dependencies.

5. Claims 1 and 2 were also rewritten as new claim 2 free of indefinite expressions like "this value" and "passing".

6. Claim 10 has been canceled.

At page 6, paragraph 3, the examiner rejects claim 10, and states: Claim 10 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by "Dynamically Changing the Logical Behavior of a Microcomputer Interface", I Dancea, IEEE Micro, April 1989. The expert system recited by Claim 10 is a piece of software which generates the necessary data used by the proposed method for reconfiguration procedure. It has the same major task when written for the software implementation of the proposed method, as it was described in the mentioned publication, or when written for the hardware implementation of the proposed method, as it is described in the patent application. Even if their real implementation is completely different, the applicant considers that this Claim 10 can be eliminated, because its main goal was disclosed in 1989. Consequently, this claim does not exist in the new formulation.

Claim rejections under 35 USC 102

Applicant's invention

The present application recites a method for implementing in reconfigurable VLSI devices, one or several combinational and/or synchronous sequential circuits with multiple outputs, having the functions expressed in sum-of–product (SoP) equations.

Today, the existing reconfigurable VLSI devices are classified in two possible architectures: Complex Programmable Logic Devices (CPLD) and Field Programmable Gate Arrays (FPGA).

Figures A, B and C are enclosed.

Architecture-1

The Programmable Logic Arrays (PLA) is the structure that generalizes, by programmability facilities, the direct implementation of the SoP form of logical equations. The input variables (in their true or complemented form) are connected to the AND gates, found in the AND plane, through individual programmable switches (usually based on EEPROM memories), which allow the selection of variables for each product term. Next, the product terms are connected to OR gates, found in the OR-plane, through programmable switches, as well. Therefore, if the same product term exists in several logical equations, this product term must be implemented only once.

A second solution, based on a simplified structure called Programmable Array Logic (PAL), has only the AND plane programmable. In PAL solution, the programmable OR array is replaced with a fixed OR gate for each logical equation, where this OR gate has connections from the AND gates that implement the product terms of the single logical equation. Consequently, in PAL solution if the same product term exists in several logical equations, this product term must be implemented a number of times by AND gates, ones in every existing equation. As it is known, structures like PLA and PAL are used as logic blocks of Complex Programmable Logic devices (CPLD).

An example of a simplified cell, in a CPLD device based on PAL solution, implementing a single logical SoP equation of a combinational circuit, is shown in the enclosed Figure A. It can be mentioned that this architecture needs a large number of programmable switches, which must be erased and reprogrammed for every implementation of new target circuit (takes usually hundreds of milliseconds) and in addition, the internal structure of the reconfigurable CPLD device changes for every new target circuit. Also, it can be observed that the AND plane is realized with gates having a very large number of inputs for a reasonable number of variables (16, 32 or 64) fact which can pose problems to electronic implementation.

Architecture-2

The Look Up Tables (LUTs) are the logic blocks of Field Programmable Gate Arrays (FPGA). A single logic equation of K variables can be implemented by a memory (usually SRAM memory) with a capacity of 2^K words of 1 bit having an address decoder, 2^K address lines and one data output line. Each combination of the address vector represents a fundamental product that contains all the input variables and can be employed to represent the corresponding minterm. Consequently, the LUT represents the implementation of the truth table of the subject logical equation. A system of N logic equations, which is defined in terms of the same input variables, can be implemented by a memory with a capacity of 2^K words on N bits, each word corresponding to a multi-bit output.

An example of a simplified cell in a FPGA device, based on LUT solution, and implementing the same single logical equation, is shown in the enclosed Figure B. This architecture is impractical to be used for large number of inputs, given that the size of memory and of the tied decoder grows exponentially with the number of variables. Usually the architecture of a FPGA contains basic blocks having LUTs of 4 or 5 inputs and connections buses with programmable switches.

New Architecture in Applicant's application

The Applicant's proposed product terms method indirectly implements in hardware the product terms of sum-of-products logical equations that define a target circuit which must be implemented in a reconfigurable VLSI device.

According to Applicant's second embodiment, the novel circuit uses two registers, as local memory, for each basic cell of a product term (similar to PAL solution in CPLD). More precisely, the first register is written with the mask word corresponding to the sum of the weights of input variables representing a product term. The second register is written with the product word representing the sum of the weights of the input variables that gives to product term the value of logic 1.

Because each product term may assume a value of 1 or 0, in order to find this value for a set of considered input variables, the method uses two steps. First, an AND masking of the input with the mask word to extract the variables of a product term gives an intermediate result. Second, using XNOR gates, a comparison of this intermediate result with the product word to determine the real value of the product term is performed. Finally, the product terms values are OR-ed to determine the function's output.

An example of a simplified cell, in a proposed device implementing the same logical SoP equation of a combinational circuit, is shown in enclosed Figure C. Compared with Figure A, it can be seen that the "new architecture" is completely different, even if the logical behavior of an implemented target circuit is identical.

The advantage of the Applicant's new architecture resides in its fixed hardware structure in the limits of parameters as inputs, outputs and product terms. No programmable switches are required and there is no need to erase these programmable switches for changing the structure from one circuit to another. The present invention requires a simple write operation in the local memory (usually a SRAM memory) for a circuit. Additional advantages follow, like the speed of reconfiguring which is higher.

In a first embodiment, each product term of a multi-output functions are characterized by three elements stored in registers. Namely, mask word, product word, and function word. Mask and product words play the same role as discussed above. The newly introduced function word represents the sum of the weights of the outputs where a product term has the value of logic 1. Because a product term may be present in several equations, the function word of an active product term is OR-ed with functions word of other active product terms to determine the outputs for given inputs.

7. Claim 1 unpatentable over US 6,034, 546 (Jones) in view of US 6,212,670 (Kaviani)

The above description of existent reconfigurable devices will be used in the following to provide arguments for overcoming Examiner's rejections.

At page 7 (paragraph 5) the examiner rejects the main Claim 1 of the application by stating: "Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,034,546 issued to Jones et al in view of U.S. Patent 6,212,670 issued to Kaviani".

Jones (U.S. Patent 6,034,546) in the "Field of the Invention" section states: "... the present invention pertains to the field of product term based simple and complex programmable logic devices, generally known as SPLDs and CPLDs, respectively". Further, in the paragraph "Summary of the invention" Jones states:"an object of the present invention is to provide a dedicated carry chain method and architecture for a programmable logic device macrocell that does not require the carry chain logic of a previous macrocell to implement an initial Carry Input other than 0. It is also an object of the present invention to provide a dedicated carry chain and a method of propagating a carry between macrocells of a product term based programmable logic device that do not depend upon a function generator to implement the carry chain, and that do not suffer from the propagation delay penalties associated with conventional arithmetic function implementations"...

The Jones's patent teaches a carry chain, which is a communication technique between cells in VLSI devices implemented in accordance with Architecture-1. Jones discloses a direct implementation of combinational circuits expressed by sum-of-product equations, having multiple cells and summing elements receiving product term values exactly

following the principles of Architecture-1. It is to be noted that, Architecture-1 is totally different from the VLSI devices used by the Applicant's New Architecture.

Kaviani (U.S. Patent 6,034,546) in "Summary of the Invention" section states: "In one general aspect, the invention features a programmable monolithic integrated logic circuit that includes look up table circuits and programmable logic array-like circuits. The plurality of look up tables can be arranged in blocks that each occupy substantially the same area as each of the programmable logic array-like circuits. The integrated circuit can include a first number of the look up tables and a second number of the programmable logic array-like circuits"... Further, in the section: "Brief Description of the Drawing" Kaviani introduces drawings having the following captions:

FIG. 1 is a simplified block diagram of an integrated circuit according to the invention;

FIG. 2 is a simplified block diagram of a LUT circuit block for use in the integrated circuit of FIG. 1;

FIG. 3 is a schematic diagram of a PLA-like circuit block for use in the integrated circuit of FIG. 1...

It is easily apparent that Fig. 2 of Kaviani illustrates a logic block of a FPGA-type device as described in Architecture-2, and Fig 3 of Kaviani illustrates a logic block of a CPLD device as disclosed in Architecture-1.

Again, these two existent architectures, namely Architecture-1 and Architecture-2, do not have any structural and/or functional similarities with the VLSI devices disclosed and claimed by Applicant according to the New Architecture.

Going further, the Examiner states: "It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teaching of Jones relating to implementing combinational circuit using sum-of-product equations, with the teachings of Kaviani relating to the use of product term cells, to realize the claimed invention".

This statement is not supported, because the applied patents disclose logical architectures which are different in structure and functionality.

The Applicant believes that the References can not be combined if their intended function is destroyed. There must be a technological motivation for engaging in the modification.

Considering the other mentioned patents and publications the conclusion is identical. Here is the analysis of other references cited by the Examiner:
Ashar et al (U.S. Patent 6,662,323) in the section "Summary of the Invention" states: "A fast error diagnosis system and process for combinational verification is described. The system and process localizes error sites in a combinational circuit implementation that has been shown to be inequivalent to its specification. The invention uses a diagnosis strategy of gradually increasing the level of detail in the analysis algorithm to ultimately derive a small list of potential error sites in a short time." This description concerns specially the fixed combinational circuits and does not have any connection with reconfigurable architectures.
Xue et al (U.S. Patent 6,091,892) in the section "Summary of the Invention" states: "A method for programming complex programmable logic devices (CPLDs) to implement a logic function, whereby user-designated locked equations of the logic function are mapped into the macrocells of a function block, and then undesignated (non-locked) equations are mapped into the remaining macrocells. The method shifts product terms between the macrocells to adjust the placement arrangement of the mapped equations, thereby obtaining a placement arrangement which is both valid and meets user-defined timing constraints". This invention concerns CPLD device as it was described for Architecture-1 and do not have any connection with the VLSI devices implemented in accordance with the New Architecture proposed by the applicant.
Steele et al (U.S. Patent 5,309,046) in the section "Summary of the Invention" states: "In a programmable logic device having a plurality of gates capable of being programmed according to a plurality of product terms representing logic functions ...."
Further, Claim 1 of this patent states: "an apparatus for allocating said plurality of

product terms to said plurality of output..."and Claim 2 of this patent states: "the apparatus of claim 1 further comprising: a plurality of AND gates coupled to said input means which can be programmed to perform AND functions on said signals according to said product terms; a plurality of OR gates coupled to said plurality of AND gates for performing OR functions on said signals after said signals have been processed by said AND gates".. Clearly, this invention concerns an apparatus and method for product term allocation in programmable logic CPLD device, as it was described for Architecture-1 and consequently this patent do not have any connection with the VLSI devices implemented in accordance with the New Architecture proposed by the applicant. The Applicant believes that the rejection under 35 USC 103 has been overcome.

Demo-Unit

The applicant had recently implemented a demo-unit of the proposed method. If the Examiner considers necessary, the Applicant can meet the examiner at his preferred place to show this demo-unit, answer questions if any, and review the differences between the existing reconfigurable architectures and the invention in this patent application.

It is respectfully submitted that the invention taught and defined herein by the revised claims embodies patentable subject matter. The Examiner is earnestly solicited to give, as always, favourable reconsideration to this application and pass it to allowance. If the Office finds appropriate, the undersigned would welcome a telephone interview to discuss any matter relating to the Amendment. As well if any additional sum of money has to be paid, the Applicant will immediately send a Certified Cheque.

Respectfully submitted,

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Claims with marked corrections

1 (Canceled)

2 (Currently amended) A dynamically reconfigurable VLSI device [circuit] for implementing in hardware any multiple outputs combinational target circuit having the output functions expressed in logical sum-of-product equations with a maximum of m inputs, a maximum of r outputs and a maximum of n product terms p(k), comprising:

a register with m bits for storing the input variables;

n cells, a cell C(k) for determining the logical value of a product term p(k) of said equations for given inputs;

[a logical summing circuit, realised with] a block of r OR gates each one with n inputs, associated with said cells C(k) for receiving the logical value of product terms p(k) and outputting the r bits of output functions[.];

wherein said cell C(k) comprises:

a storage area for storing the information that characterizes a product term, named mask word, product word and function word;

first logic level [AND gates] means for receiving said m inputs and said mask word to produce a first intermediate result, which identify the input variables that form a product term;

second logic level [EQUIVALENCE gates] means for comparing the said product term with said first intermediate result to produce a second intermediate result concerning a product term;

third logic level [second AND gate] means for receiving [the] said second intermediate result to produce [a] the logical value [which is the value] of the product term; and [if this value is logical 1 the product term is active;]

forth logic level [third AND gates] means [to allow passing] for transferring said function word to r outputs, according to said logical value of said product term p(k), [if said product term is active] and [consequently] subsequently to be OR-ed with function words of other [active] product terms.

3 (Currently amended) A dynamically reconfigurable VLSI device [circuit] as in claim [1]2, wherein said storage area of a cell C(k) comprises two m-bit registers and one r-bit register. [for m input bits of said C(k) cell.]

4 (Currently amended) A dynamically reconfigurable VLSI device [circuit] as in claim [1]2, wherein said first logic level [AND gates] of a cell C(k) comprises m*(2-bit) AND gates each one for receiving a respective bit of said m input variables and of said mask word [for m input bits] to produce said first intermediate result. [as in claim **2** and in claim **12**]

5 (Currently amended) A dynamically reconfigurable VLSI device [circuit] as in claim [1]2, wherein said second logic level [EQUIVALENCE gates] of a cell C(k) comprises m*(2-bit) [EQUIVALENCE (]XNOR[)] gates each one for receiving a respective bit of said first intermediate result and of said product word to produce a bit of [for m input bits] said second intermediate result. [as in claim **2** and in claim **12**]

6 (Currently amended) A dynamically reconfigurable VLSI device [circuit] as in claim [1] 2, wherein said third logic level [second AND gate] of a cell C(k) comprises one m-bit AND gate [for m input bits] to produce a logical value which is the value of the product term. [as in claim **2** and in claim **12**]

7 (Currently amended) A dynamically reconfigurable VLSI device [circuit] as in claim [1] 2, wherein said forth logic level [third AND gates] of a cell C(k) comprises m*(2-bit) AND gates [for m input bits to allow passing] for transferring said function word to outputs, considering the logical value of said product term p(k). [if said product term has the logical value of 1.]

8 (Currently amended) A dynamically reconfigurable VLSI device [circuit according to claim **1**] for implementing in hardware any target synchronous sequential circuit with clock input only and outputs taken from the state register, [having the next state functions expressed in logical sum-of-product equations with s bits in state register and n product terms p(k),] further comprising:

[a clock input;]

a state register with s bits for storing the state variables;

a combinational part implemented as described in claim **2**, expressing the next state functions in logical sum-of-product equations, with a maximum of s inputs and outputs, and a maximum of n product terms p(k); and

[n cells of said cell C(k) for determining the logical value of a product term p(k) of said next state equations;]

[a logical summing circuit, realised with s OR gates each one with n inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) and outputting the s bits of said next state functions;]

a feedback connection to establish the next state.

9 (Currently amended) A dynamically reconfigurable VLSI device [circuit according to claim **1**] for implementing in hardware any synchronous sequential circuit with clock input and data inputs, [having the next state functions and the output functions expressed in logical sum-of-product equations, with m inputs, r outputs, s bits in state register, n1 product terms p(k) in next state equations and n2 product terms p(k) in output equations,] further comprising:

[a clock input;]

a register with m bits for storing the input variables;

a state register with s bits for storing the state variables;

a first combinational part which is implemented as described in claim **2**, expressing the next state functions in logical sum-of-product equations, with a maximum of m+s inputs, a maximum of s outputs, and a maximum of n1 product terms p(k);

a second combinational part which is implemented as described in claim **2**, expressing the output functions in logical sum-of-product equations, with a maximum of s inputs, a maximum of r outputs, and a maximum of n2 product terms p(k); and

[n1 cells of said cell C(k) for determining the logical value of a product term p(k) of said next state equations;]

[n2 cells of said cell C(k) for determining the logical value of a product term p(k) of said output equations;]

[a logical summing circuit, realised with s OR gates each one with n1 inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) of the next state equations and outputting the s bits of next state functions.]

[a logical summing circuit, realised with r OR gates each one with n2 inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) and outputting the r bits of output functions.]

a feedback connection to establish the next state.

10 (Canceled)

11 (Canceled)

12 (Currently amended) A dynamically reconfigurable VLSI device [circuit as defined in claim 1, wherein if said VLSI circuit has one output (r=1), said cell C(k) comprises:] for implementing in hardware any multiple-output combinational target circuit defined by a group of logical sum-of-product equations with maximum of m inputs, maximum of r outputs and a maximum of q product terms in each equation, having a register with m bits for storing the input variables and for each single sum-of-products logical equations, considered as an independent equation, further comprising:

q modified cells, a modified cell C(k) for determining the logical value of a product term p(k) of said independent equation, for given inputs;

a single OR gate associated with said q modified cell C(k) for receiving the logical value of product terms p(k) to provide a single output for said independent equation;

wherein said modified cell C(k) comprises:

a storage area formed by two m-bit registers for storing the information that characterizes a product term, named mask word and product word;

first logic level that comprises m*(2-bit) AND gates, each one [means] for receiving a respective bit of said inputs and of said mask word to produce a respective bit of [a] first intermediate result, which identify the input variables that form a product term;

second logic level that comprises m*(2-bit) XNOR [EQUIVALENCE] gates, each one for receiving a respective bit of [and means for comparing the] said product word [term with] and said first intermediate result to produce a second intermediate result concerning a product term; and

third logic level [second] that comprises one (m-bit) AND gate [means] for receiving the m bits of said second intermediate result to produce a logical value which is the value of the product term.

13 (New) A dynamically reconfigurable VLSI device for implementing in hardware any target synchronous sequential circuit with clock input only and outputs taken from the state register, further comprising:

a state register with s bits for storing the state variables;

a combinational part implemented as described in claim **12**, expressing the next state functions in logical sum-of-product equations with a maximum of s inputs and outputs, and a maximum of q product terms p(k) in each considered sum-of-product independent equation; and

a feedback connection to establish the next state.

14 (New) A dynamically reconfigurable VLSI for implementing in hardware any synchronous sequential circuit with clock input and data inputs, further comprising:

a register with m bits for storing the input variables;

a state register with s bits for storing the state variables;

a first combinational part which is implemented as described in claim **12,** expressing the next state functions in logical sum-of-product equations with a maximum of m+s inputs,

a maximum of s outputs, and a maximum of q1 product terms p(k) in each considered independent sum-of-product equation;

a second combinational part which is implemented as described in claim **12,** expressing the output functions in logical sum-of-product equations with a maximum of s inputs, a maximum of r outputs, and a maximum of q2 product terms p(k) in each considered independent sum-of-product equation; and

a feedback connection to establish the next state.

15 (New) A method for implementing in a dynamically reconfigurable VLSI device a target circuit selected from multiple-output combinational circuits and synchronous sequential circuits defined by groups of sum-of-product logical equations, in limits imposed by the parameters number of inputs, number of outputs and number of product terms, the method comprising the steps of:

inputting a request to reconfigure said VLSI device to said target circuit;

identifying the VLSI device to be configured, considering its internal structure of cell C(k) as described in any one of claims **2** or **12**;

generating memory words uniquely defining each product term p(k) of said sum-of-products logical equations; and

implementing the target circuit by storing each said memory words into a corresponding register of a cell C(k) as defined in any one of claims **2** or **12**.